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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 15

Application Number: 08/654,760
Filing Date: 5/29/96
Appellant(s): Vora

Ronald Craig Fish
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 8/5/98.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief contains a statement that there are no other related appeals or interferences.

(3) Status of Claims

The status of the claims remains as stated in the final Office action. Appellant submitted an after final amendment on 6/12/98, but did not label this amendment as an after

final amendment, as required by MPEP 714.13. Consequently, this amendment did not receive expedited processing, as Appellant apparently expected that it would, and did not reach the examiner until after Appellant's Brief had been filed. Appellant also had a paper labeled "Supplemental Response" hand carried to the examiner on 6/17/98, but the person who carried the paper in refused to get a date stamp, stating that the paper was "informal only, not to be entered." Examiner told Appellant's representative by telephone that the informal paper would not overcome the final rejection, and that the claim amendments contemplated were apparently new issues, but that a formal response could not be given on the record until the examiner received the complete response, and in something other than an informal paper. Appellant apparently expected to receive an Advisory Action, or some other formal paper, in response to his hand carried paper, but PTO procedure does not contemplate acting on an applicant's *informal* submissions. When the formal copies of the papers submitted on 6/12/98 and 6/15/98 were received by the examiner, a formal response was entered as Paper 13. (Examiner suggests that all after final amendments be labeled as such, and also suggests that hand carried papers be submitted to the receptionist for date stamp, if a formal or written response is needed.)

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. See the discussion under (3) above.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct. The underlining and deletions are the same as in the previous amendment, and do not reflect additions or deletions made after the final rejection. (Examiner suggests that underlining and deletions are not necessary in the copy of the claims submitted for appeal.)

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,071,782	Mori	Dec. 10, 1991

(11) Grounds of Rejection

Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Mori.

Mori teaches in figure 1 a memory cell array comprised of a plurality of nonvolatile memory cells. Figures 1a and 1b show the structure of the cells. The drain regions are 24, formed in the p-type substrate and having a surface along the well "coincident suitable to act as a drain region." (The "substrate" is identified as all the p-type layers or regions of the device, contiguous with the "p substrate" as shown in figures 1a and 1b. Although the drain region is "formed in" the substrate, once formed it is n-type, and is therefore not considered part of the p-type substrate.) The buried layer channel is shown at 25 extending under the drain vertically along the edge of the trench. The channel is p-type, and the drain is n-type. The source region is the n-type region under the channel region. The recessed gate is in the form of a well etched in the substrate and extending through the insulating layer on the top of the substrate. An insulating layer covers the bottom of the well and a gate insulator layer adjacent the channel is on the sidewall of the well. Floating gate FG is "self aligned . . . so as to not extend beyond the edges of said well," because FG does not extend beyond the edges of the well.

"Self alignment" refers to a process limitation in which alignment between device regions, usually gate/source and gate/drain alignment, occurs by itself, i.e., without the necessity of a mask alignment step. A process limitation carries weight in a claim drawn to a product only to the extent that the recited process step necessarily gives rise to structure distinct from that of the prior art. *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985); see also cases cited therein. Moreover, burden is on *applicant* to present evidence that the recited

process limitation necessarily gives rise to distinct structure. In this claim, the process limitation "self aligned" would not give rise to distinct structure because the Mori gate FG aligns with the Mori source and drain regions by itself, as a result of filling in the well region with the FG material, without the necessity of any particular up/down alignment step to determine placement of FG relative to source and drain. Moreover, Appellant has presented no evidence to the contrary.

Insulating layer ILO is over the floating gate FG as recited, and FG has a dimension suitable so as to overlie the channel. Word line PG (or WL as in figure 3) extends into the well to overlie FG. The "second layer of insulating material" is read on the diagonally-lined layer extending from ILO to cover the underlying insulating layer, which insulates at least a portion of the word line.

The bit line is that part of buried region 34 that does not function as the drains of the cells, which extends between the cells as shown by "BL" in figure 3, and which is formed over the surface of the p layer(s) identified above as the p-type substrate. The buried bit line is insulated from the word line by both insulating layers.

Claims 1 and 3-4 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103, as obvious over Mori.

With respect to claim 1, each element would be identified exactly as noted with respect to claim 2 above, with the "bit line contact" being read on the diffused bit line 34 (which is a

layer on conductive material formed on the p-type substrate so as to be in electrical contact with the drain region of each cell). Alternatively, it would have been obvious to provide a "contact" to the buried bit line at 34a, on the right side of figure 1a, because that is why the hole at 34a is provided. Such a contact would be in electrical contact with each drain region along the bit line through the buried bit line 34.

With respect to claims 3-4, the regions are identified as above. The "first layer of N-type conductivity" is identified with the part of Mori layer 34 that functions as a drain region as required by claim 3 ("a first layer of N-type conductivity . . . forming a drain region"). The "bit line" is identified with that part of Mori layer 34 that extends between the cells, necessarily "on the surface of said substrate so as to be in electrical contact with the surface of said first layer coincident with the surface of said substrate at each cell."

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori.

The embodiment of figure 2a in Mori teaches to have a drain contact area for each cell in the column (column 6, lines 6-8), instead of a buried bit line with a single contact at the end of the row as shown in figures 1a and 1b. A drain contact line is formed over the drain contact areas along each bitline row (column 6, lines 16-20). It would have been obvious to include a "spacer layer" of insulating material insulating between such a drain contact line and underlying word line contacts, because otherwise the bitlines and the wordlines would be shorted out.

Claims 1-2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, line 4, it is unclear with what the "surface" is coincident; in line 34, it is unclear from what the word line is being insulated, or where the second layer is located.

In claim 2, line 4, and in claim 3, line 5, it is unclear how a surface (a two dimensional entity) can act as or form a drain region, which conventionally is a three-dimensional entity, such as a portion of a layer having a thickness.

In claim 3, lines 22-23, the "word line contact" and "bit-line contact" lack antecedent basis.

(11) Response to Argument

Self-aligned

Appellant states that the Board should take judicial notice of the fact that people skilled in the art understand the term "self aligned" in integrated structures to mean "formed without using a mask" (Brief page 12, lines 12-16). Examiner urges that "self aligned" does ***not*** mean "formed without using a mask." Self-aligned means what it says and nothing more, i.e., alignment which arises by itself, without the necessity of a mask alignment step. Device

structure may in fact be formed using a mask, and there may even be a mask alignment step, but the alignment of the structures referred to as "self-aligned" comes about by itself, and not as a result of mask alignment.

Moreover, the burden is on the applicant to provide evidence that a process limitation, relied upon for patentability in a product claim, necessarily gives rise to distinct structure. Appellant has provided no evidence at all here, relying only on arguments intended to convince the Board to take "judicial notice" that the claim language means something other than what it plainly states. Examiner suggests that this would be reading a limitation into the claim which is not required by the claim language. Moreover, this limitation is not even described in the specification, which does not refer to a self aligned floating gate anywhere. (What is self aligned is the memory cell, as noted in the heading of the table on page 13 of the specification.) Moreover, the specification does not even describe a process for making a floating gate that does not use a mask. The process of forming the gate could be performed with or without a mask, and the specification is silent on this point. Appellant cannot rely on any definition of "self aligned" set forth in the specification, because there is none.

Appellant also apparently argues that the Mori floating gate would extend laterally beyond the edges of the well, even though the figure does not show this. Examiner can see no reason why the device as taught by Mori could not be fabricated with the gate dimensions exactly as shown. Whether a mask is used or not, the dimensions of the well and the gate can be chosen independently.

Bit lines on the surface of the substrate

The examiner understands that the buried bit line of Mori figures 1a and 1b would meet the claim limitations, because the n-type buried layer 34 extends on the surface of the underlying p-type layer, which is itself identified as substrate. The embodiment of Mori figures 2a and 2b covers the situation where a separated bit line, separated from the substrate, extends above the device layers and contacts each cell at the location of the cell. Appellant urges that "formed on said substrate" as in claim 1, or "formed over the surface of said semiconductor substrate" as in claim 2, must be read as "separated from the substrate." Examiner disagrees, but even if the language is interpreted in this fashion, Mori teaches to do exactly this.

Declaration of Vora

The following is repeated from Paper 13, which treated the declaration:

The Declaration of Madhukar Vora, submitted 6/12/98, is not convincing because it discusses advantages of the process disclosed in the specification, such as a small cell size and improved alignment tolerance. The claims are not limited to devices having the noted advantages, however, and no limitations on cell size or alignment tolerance appear to be even recited in the claims.

Applicant argues that the examiner has improperly construed the claim limitation "self aligned" as used in for example claim 1 to describe the floating gate. The claim language has been

properly construed under the broadest reasonable interpretation standard required for claim construction by an examiner. MPEP 2111. The examiner has construed the claim limitation "self aligned to not extend laterally beyond edges of said well" to mean that the floating gate does not extend laterally beyond edges of the well, and is aligned adjacent to the source, drain, and channel of the vertical transistor. This is the plain meaning of the claim language, and the specification does not provide any clear definition to the contrary. See MPEP 2111.01.

The examiner has also noted that "self aligned" is a processing limitation, which carries weight in a claim drawn to structure *only* to the extent that distinct structure *necessarily* results from the recited process. *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985). Burden is on Applicant to provide evidence that the process step(s) relied upon for patentability necessarily give rise to distinct structure. Applicant has presented no evidence to provide this showing, and the examiner has therefore given no weight to the claim terminology "self aligned" beyond the plain meaning interpretation noted above.

Applicant presents attorney arguments to urge that "self aligned" means that the floating gate is made by steps 33 and 34 as described on page 14 of the specification, and that these process steps would give rise to a structure with no poly on any horizontal surface. These arguments are not convincing to the examiner because interpretation of the claim language in this manner would be an improper reading of limitations from the specification into the claims.

Note first of all that the specification does not refer to the floating gate as self aligned. Rather, it is the memory cell itself that is taught as self aligned, not the gate (specification, page 13, line 10).

Also, "self aligned" is a term of art used to describe device structures for which alignment arises in some manner naturally from the processing steps, rather than by a separate alignment step in the process of making. The term is used in the context of vertical channel transistors to indicate that a gate electrode deposited within a groove or trench aligns naturally with source/drain regions at the top and bottom of the groove or trench, because the gate electrode extends along the edge of the groove or trench, without need for any particular gate electrode up/down alignment step. This type of alignment is shown in the prior art of Mori used to reject the claims, although alignment which occurs without a separate alignment step would appear to give rise to identical structure as alignment which occurs with a separate alignment step. (In either case, one ends up with aligned structures.) Because the process limitation of "self aligned" does not give rise to any device structure that is necessarily different or distinct from a process including an alignment step, the limitation would not carry patentable weight. If patentable weight were, however, to be given to the limitation, the structure resulting from a processing step of "self alignment" would be indistinguishable from the prior art structure.

Furthermore, the process steps 33 and 34 in the specification do not say anything about removing all poly from horizontal surfaces. Step 34 says merely to etch back from horizontal

surfaces, which means to etch *from* a horizontal surface, i .e., straight down, for example. One may or may not end up with all poly removed from horizontal surfaces.

Appellant urges throughout the Brief that claim language be construed in such a manner as to avoid the Mori reference. However, claims should be construed to mean what they state and nothing more. Claims should be amended, not construed, to avoid references. *Briggs v Lillie v Cooke v Jones and Taylor*, 1905 CD 158.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Sara Crane
Primary Examiner

November 9, 1998